WG#1: Alg. Spec. Arch./Adaptive Computing

Report Summary

- **Problem Description / Technical Scope**
  - Computing with adaptive HW. Effectively merging programmable processors with flexible HW
- **Relevant Disciplines / Technologies**
  - Commercial FPGA vendors, SW design/translation, sensor processing
- **Major Technical Challenges**
  - Data-dependent reconfiguration, tools, new architectures, programming models, redesigning algorithms to exploit adaptive HW, variable precision arithmetic

Addressing the Challenges

- Data dependent reconfiguration: domain-specific parameterized libraries
- Accelerating DSP applications: Coarser grained structures, new architectures, reconfigurable interconnect
- How to redesign algorithms to exploit adaptive HW: Provide hardware-aware abstraction to algorithm designer
- Efficient utilization of HW: adaptive precision

Projected Outcome

- 10-100x acceleration on ATR and other sensor processing
- Drive FPGA vendors to better architectures and support for dynamic configuration
- Fault tolerant and threat-adaptive circuits
- Dedicated circuit design cycles in days instead of months
- Ability to field upgrades/revisions to HW - lower costs

WG#1: Alg. Spec. Arch./Adaptive Computing

Investment Strategy

- **DARPA, Industry Support**
  - Why DARPA? - industry is not investing/innovating in this area (current market is emulation, glue logic; no incentive to invest outside this area)
  - **Other collaborations? -** mil./comm. end users, genl computing community (compilers, HW/SW codesign), FPGA vendors
- **What if we did not do this?**
  - Less capable military systems
  - Lose technological lead to foreign competition
  - Dimished access to dedicated HW efficiencies
- **Optimal Scale of Efforts**
  - In short term need to explore multiple architectures, approaches; should narrow focus several years out